ATX7006

Setting up an A/D converter linearity measurement

This application note describes how to setup a simple A/D converter measurement using the ATX7006 in combination with the application program ATView.

The ATX7006 is designed to setup A/D and D/A converter measurements with ease, achieving uncompromised measurement results. In this application note, a test setup for a 12 bit A/D converter is discussed.

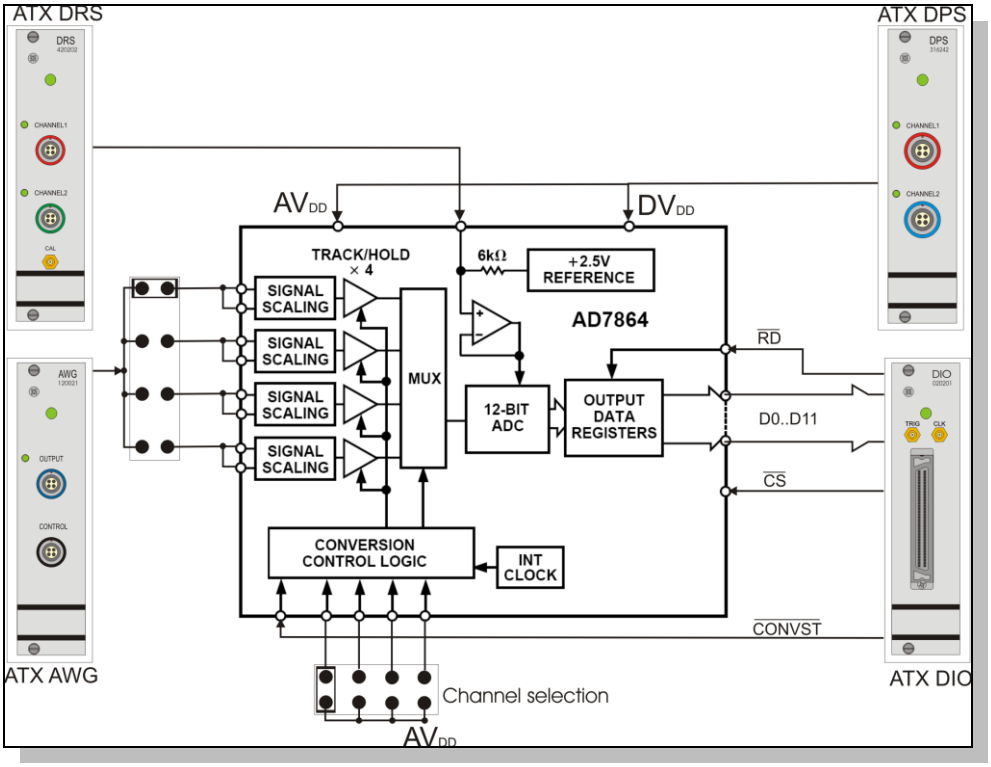
The converter

The converter to test is the AD7864, a four channel, 12 bit A/D converter from Analog Devices with a 1.65us sampling speed. The device input range is hardware selected and set to +/- 5V. The device has an internal 2.5 Volts reference. Optionally, an external reference can be used. The A/D converter channel is selected by means of a simple jumper setting.

The device has a 12 bit parallel output, controlled by $\overline{RD}$ and $\overline{CS}$. The conversion is started with $\overline{CONVST}$.

Hardware setup

The figure shows a simplified schematic of the measurement setup.



The channel under test is selected by means of two jumpers. The software channel selection option of the device is therefore not used. The input voltage is generated by the ATX7006 AWG20 module. The reference can be connected to the ATX reference module. The device is powered using one channel of the ATX7006 dual power supply module.

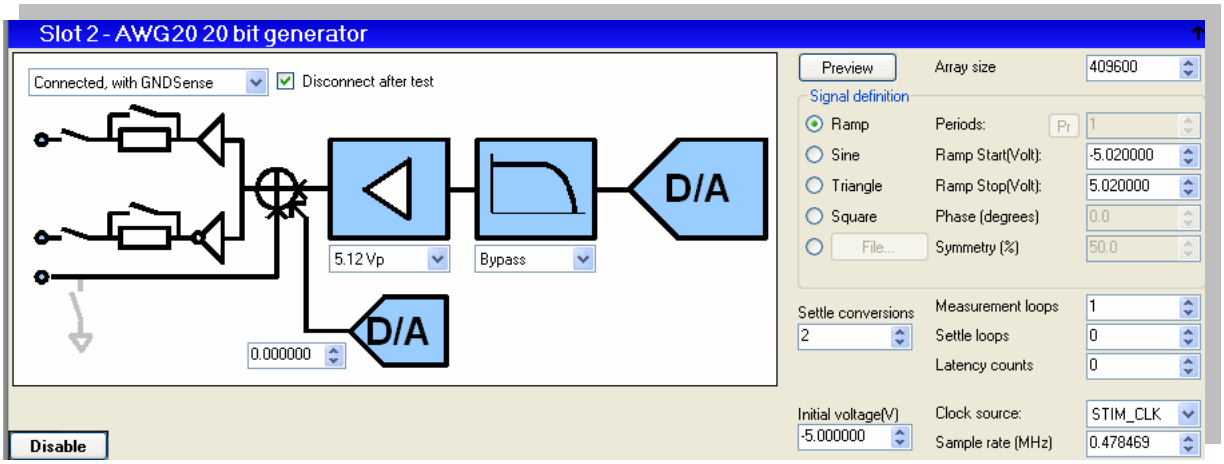
The data output and digital control lines are directly connected to the DIO module. The control lines are generated by the DIO module. For the ease of this example, the device uses its internal clock circuit.

Setup of applied test signal

To perform a linearity test, a ramp signal is applied. The signal ramps up from a voltage just below the minimum input voltage to a voltage just above the maximum input voltage. The ramp start voltage is set to -5.02Volts, and the ramp end voltage is set to +5.02 Volts. The chosen AWG20 range is 5.12Vpeak. In this range, the maximum resolution step is 9.76uV.

The number of steps of the applied ramp is high, for canceling out noise and to increase measurement resolution. In this example, the ramp resolution is a factor 100 higher than the converter resolution: $100*2^{12}$ = 409600 steps. The ramp gets a resolution step of approx. 24uV for each step.

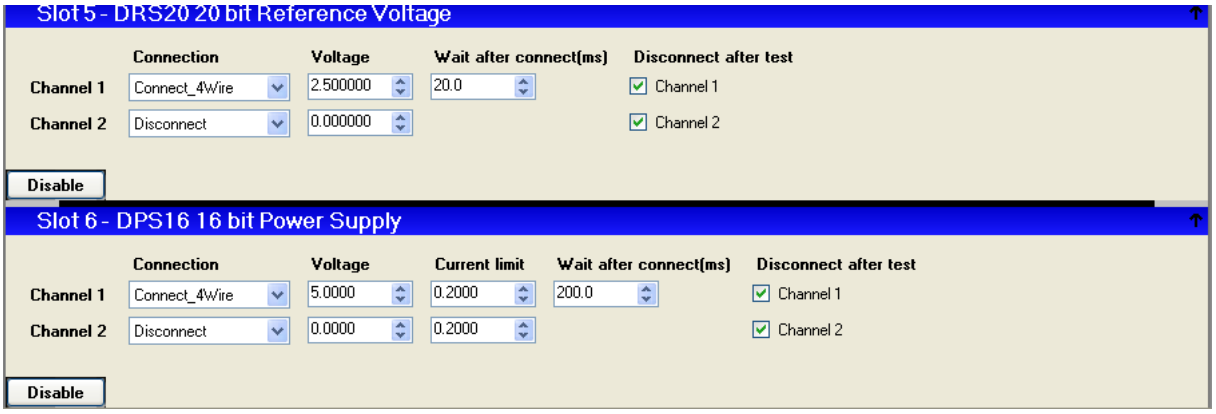
The ramp definition in ATView now looks as follows:



In connection with the high ramp resolution, additional averages are not needed. When needed, the number of measurement loops, or the number of ramp steps may be increased.

Setup reference and power supply

The dual reference DAC module and Dual power supply module are configured simply in the ATView measurement setup window.

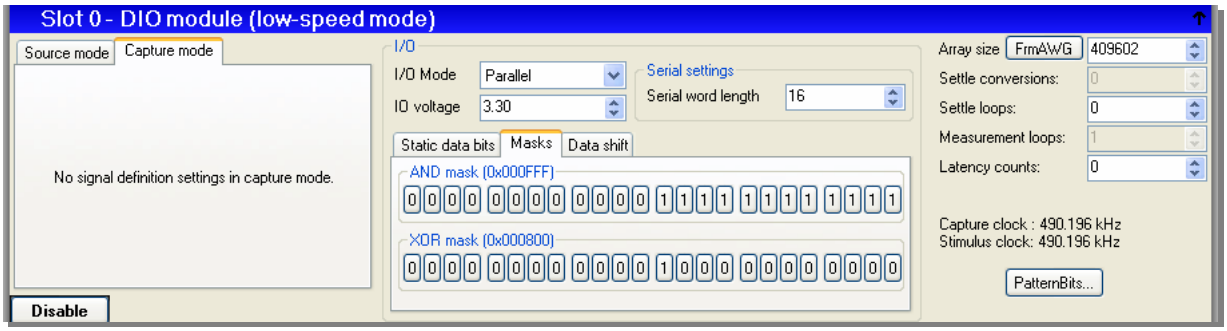


The reference voltage is set to 2.50 Volts and is 4-wire connected to the test board. The Power supply voltage is set to 5 volts and is 4-wire connected as well. The settling times are set to 20ms and 200ms respectively.

Setup of the digital IO

Data masks

The device data is 12 bit, the 12 most significant bits of the DIO capture memory are not used and can be forced to a logic low state using an and mask. In the AND mask, the used bits are set to logic high. The output data has a two's complement data format. To capture the data in straight binary format, the most significant bit is inverted using an XOR mask.

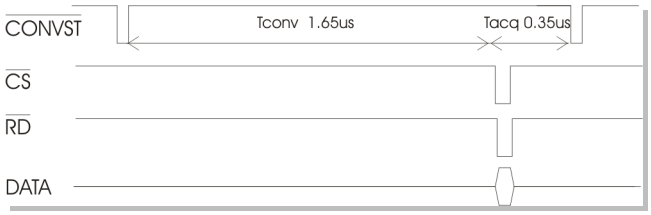


Array size

The array size defines the number of samples that are actually captured. The captured data should include the settle conversions and should cover all applied measurement loops. The setting can easily be derived from the generator settings by clicking "FrmAWG" button.

Measurement timing

The conversion starts on a positive edge of $\overline{\text{CONVST}}$. After 1.65us, the conversion is ready and data is read taking $\overline{\text{RD}}$ and $\overline{\text{CS}}$ low. After a 0.35us acquisition time, the next conversion can start.



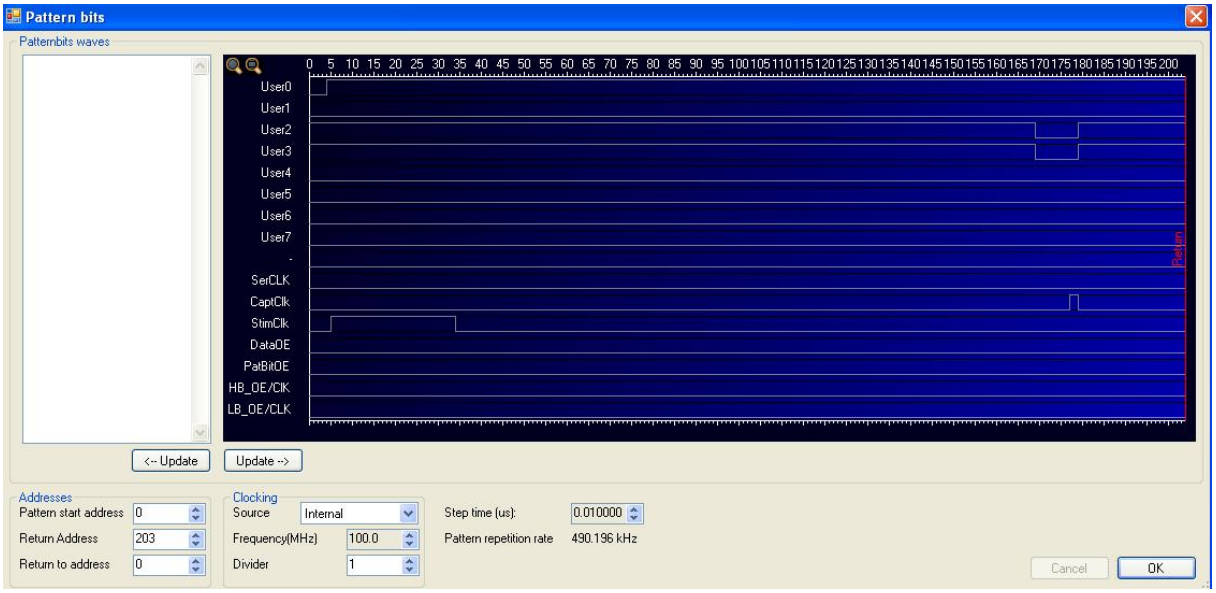
During the acquisition time the sample and hold is acquiring the analog input. The output of the AWG20 module is settled a considerable time when it is sampled right after a conversion start.

$\overline{\text{CONVST}}$ is connected to the patternbit generator bit 0, called "User0".

Likewise, $\overline{\text{RD}}$ is connected "User1" and $\overline{\text{CS}}$ to "User2".

The timing is easily programmed in the DIO patternbit generator. The timing is graphically edited in the Patternbit editor and is finished in just a few mouse clicks.

With a 10 ns pattern step resolution, the whole pattern takes 204 steps.



First, Convst is held low for 40ns. Then, after 165 steps (1.65us), the chip select and read lines are taken low to read out the converter result. The capture clock (CaptClk) stores the data into the capture memory. The positive edge of Stimclk, right after Convst, updates the AWG20 module.

Before the measurement can be started, the device under test parameters are defined. The minimum and maximum input voltages and the number of device bits are set. Besides, the DIO is selected as measurement data source.

Analysis of the measurement results

In the ATView WaveAnalyzer tool the Results of the linearity measurement can be analyzed.

The figure shows a screenshot of the analyzer software, showing the endpoint representation of the converter.